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Technical Report—Study Service Contract

TASK 1: IDAPS SYSTEM DESCRIPTION

Image Processing Technical Laboratory
Image Processing Systems Division

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The following technical report describes the physical configuration and components used in the Image Data Automated Processing System (IDAPS) being built for Eglin AFB by ERIM. This system is intended for manual Graphic Attitude Determination System (GADS) processing functions.

This document has been referenced in other reports as IPTL-88-029.

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SECTION I

INTRODUCTION

1.1 IDAPS Background

This document describes the physical configuration and components used in the image processing system referred to as IDAPS (Image Data Automated Processing System). This system was developed by the Environmental Research Institute of Michigan (ERIM) for Eglin Air Force Base.

The system is designed to perform manual (operator controlled) GADS (Graphic Attitude Determination System) processing and will serve as a baseline system designed for future enhancements to perform automatic GADS processing and other manual and automated image processing tasks. GADS image processing entails aligning a 2-D projection of a 3-D model of an object with a planar image of the actual object captured on film. In the manual GADS system the operator aligns the model to the object image by moving the model overlay on a monitor screen and visually aligning it with the object image on the screen. Once the model has been aligned to the image of the object, six parameters indicating the position and orientation of the object are obtained. This positional data is then stored in a file for subsequent processing.

This document's purpose is to describe and detail a system implementation of a set of functional specifications. The functional/performance specifications that define this system implementation are contained in companion ERIM Document No. IPTL-88-028 'IDAPS Baseline System Specifications'.

1.2 Document Organization

The following sections of this document describe IDAPS and its components in detail, grouped by major subsystems. Section II provides the System Overview. Section III describes the Input and Output components of the system. The Graphics Subsystem is outlined in Section IV. Section V details the Image Processing Subsystem. Section VI describes the Host Computer that runs the application program and directs the system. Finally, Section VII lists the system's overall mechanical, electrical, and environmental specifications.

SECTION II

SYSTEM OVERVIEW

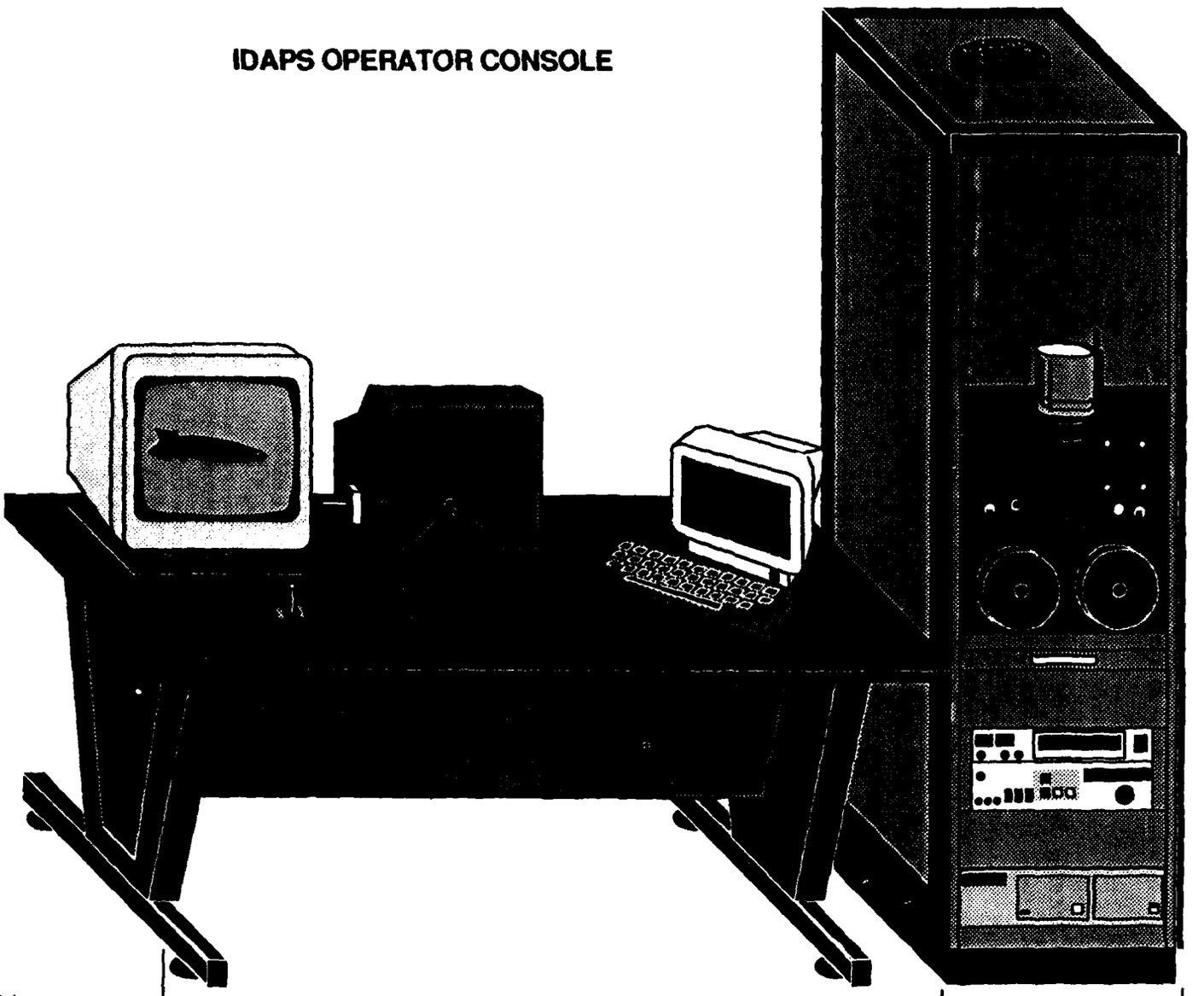
IDAPS is designed to be a versatile and extensible image data reduction and analysis system. It provides the tools and environment for performing varied and difficult image processing and analysis tasks. Experimentation, algorithm development, and production processing are all facilitated with a core system consisting of ERIM's Cyto-HSS Image Processing Workstation with C4PL, a high-level image processing language, and various attached processors and I/O devices for image acquisition, display, and additional processing.

The initial application developed for IDAPS is a filmed data reduction system. This application (Graphic Attitude Determination System, or GADS) dictated the initial configuration for IDAPS consisting of a film transport and camera for obtaining digitized images, the image processing workstation, a high-resolution display and graphics processor for image and model display, additional peripherals for image I/O and operator input, and a host computer that has overall control of the system and runs the application software.

A brief description of the operational scenario for GADS will provide an overview of the system. The GADS operator runs the application program from the host computer terminal. Film to be processed is loaded on the transport. The operator provides initialization data and directs the system to move the film to the first frame to process. A wire-frame model of an object is presented on the high-resolution monitor, along with the digitized (and optionally processed) image of the object obtained from the film. The operator moves and orients the model projection with the joysticks to line up with the object image. After a suitable match is obtained, a command is given causing the model position to be stored to a file on the host computer, and the film to step to the next frame. This process is repeated for each film frame to be processed. The end result of this process is a file of position data for the object, stored on the host computer disks. This file may then be further processed or analyzed on the host computer, or off-loaded to another computer.

The system is housed in one 19 inch electronics rack, with the host computer, film transport and camera, and a VCR accessible from the front. An operator's console is placed next to the rack. Figure 1 shows this system configuration. Functionally, the system is interconnected as diagrammed in Figure 2. All components reside in the electronics rack except the monitors, host computer console, joysticks, and the RGB to NTSC converter box, which are placed on the system operator's desk.

IDAPS OPERATOR CONSOLE



Colors:
Frames = Satin Black
Panels = Royal Blue
Table Surface = Medium Walnut

Console Rev 12
6/24/88

Figure 1

IDAPS FUNCTIONAL INTERCONNECT

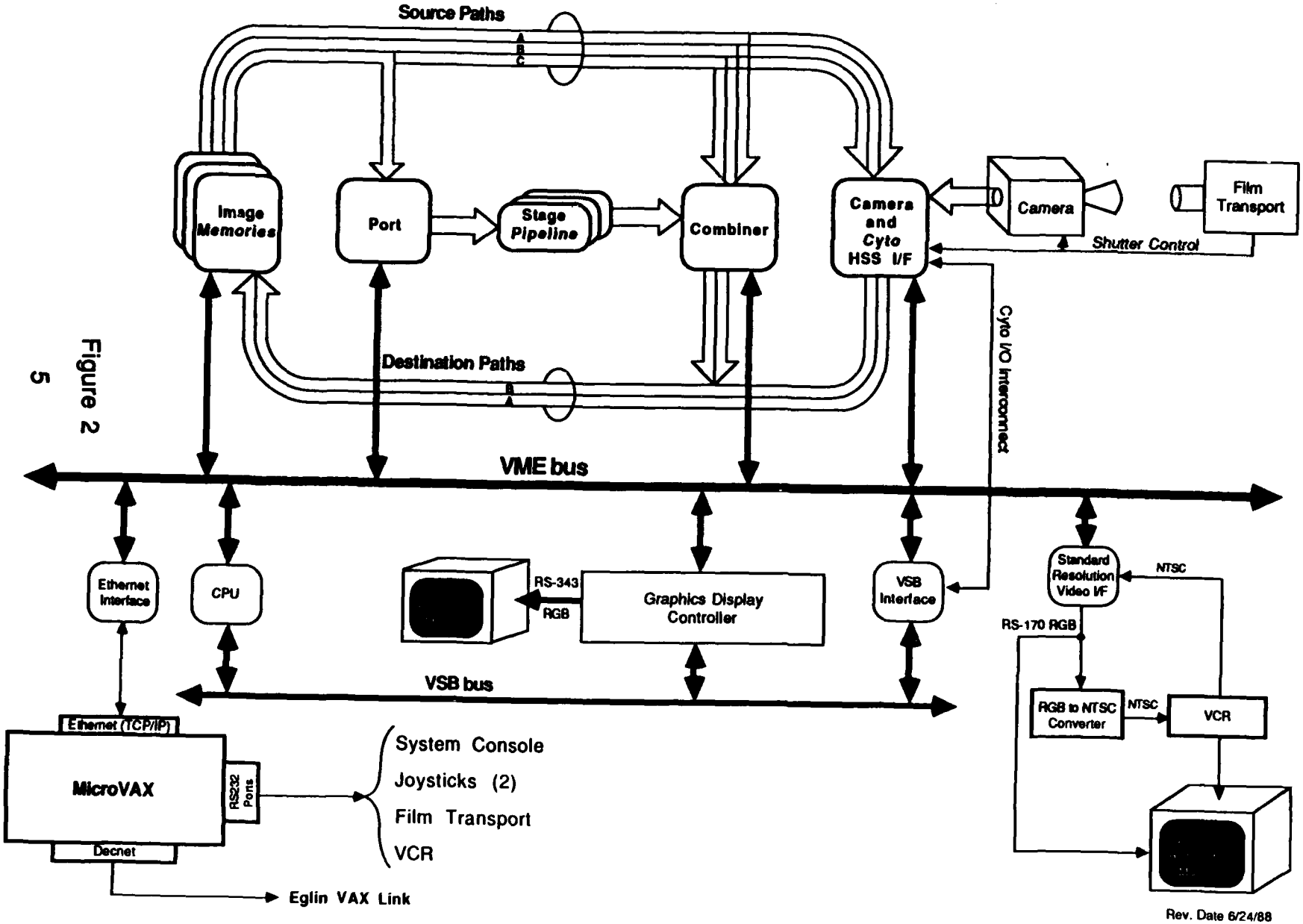


Figure 2

SECTION III

INPUT AND OUTPUT

For the GADS application a film transport and high-resolution camera are provided for digitization of filmed imagery. The camera output is directly interfaced to the image processing subsystem for input of this image data. Display of these images is provided by a high-resolution color monitor. Images and image sequences may be recorded with a U-matic format Video Cassette Recorder (VCR), and image frames may be digitized from VCR tape. Standard resolution (RS-170) video input and output is provided, primarily for interfacing to the VCR, and a second color monitor is provided for display of RS-170 RGB or NTSC video. Joystick controls for operator manual input are provided. Primary operator I/O and command of the system is provided via the host computer console terminal and keyboard.

In the following sections the film transport, camera and camera interface to the image processor, the high-resolution display monitor, the VCR, the standard resolution display monitor and display controller, the model manual controls (joysticks), and the host computer console are described.

3.1 Film Transport

The film transport in IDAPS is made by Mekel Engineering, Inc. This transport positions the film frame in the gate with high-accuracy. A custom base plate was fabricated for ERIM to provide mounting area and bolt holes for the camera. Different film formats are accomodated by interchangeable film gates. Gates for 16mm and 35mm are provided. Film must be loaded and threaded manually. Illumination is provided, with the lamp brightness manually adjustable. The light is reflected with a mirror through the film gate to minimize heat buildup around the film.

Film movement is controlled via an RS-232 port. Commands may be sent to this port to advance the film one frame, in either direction. Each advance command results in a message back from the transport to indicate that the film is stepping. Fast film movement is accomplished with repeated advance commands. Maximum film speed is approximately 15 frames/second. Fast film winding may be performed if the film is threaded around the film gate. Buttons are provided to wind the film in either direction.

A pull-out shelf is provided in the rack directly underneath the transport for convenience when mounting film reels.

3.2 Camera and Camera Interface

A Kodak Videk high resolution CCD camera is used to produce a digital video image of the film frame. A mounting plate with a high-accuracy translation stage is provided on the transport plate to position the camera for the proper magnification and focus for different film formats. This camera has a maximum usable resolution of 1035 lines of 1320 pixels. No linearity distortions or drift problems are present in this camera since it utilizes a solid-state sensor.

The CCD is an integrating sensor which requires a shutter to control exposure. Control of the shutter is provided via a parallel digital communications port on the camera. The camera provides digital video data on this port. Analog video is also available from the camera, but is not used in IDAPS.

The digital video from the camera is received and moved into the image processing subsystem via an ERIM designed interface. This interface controls the camera shutter. A status line from the film transport is also monitored by this interface to synchronize the camera shutter control with film frame stepping.

3.3 High-Resolution Display

A Mitsubishi 19 inch diagonal measure high-resolution color monitor provides the primary image output for the system. For the GADS application, this monitor displays the digitized film image with the wire-frame model overlays.

The video format supported by this monitor is RS-343. This is a 60 Hz, non-interlaced format. Resolution up to 1024 lines of 1280 pixels is provided. The video input is RGB analog video with sync on the green channel.

The graphics/display subsystem drives the high-resolution monitor. See section IV for a description of this subsystem.

3.4 VCR

A Sony VO-9600 Video Cassette Recorder (VCR) is integrated in IDAPS for image input and output, and demonstration purposes. NTSC analog video is accepted and produced by this unit. The NTSC output is available to drive the standard resolution monitor for video display of recorded material. This output can be fed into the standard resolution acquisition/display board in the image processor for digitization.

The standard resolution acquisition/display board housed in the image processor provides an analog RGB video output. An RGB to NTSC converter (external to the IDAPS rack) encodes this analog RGB signal into an NTSC signal suitable for recording on the VCR.

Computer control of the VCR is provided by a Sony BKU-701 RS-232 serial interface module installed in the VCR. The IDAPS host computer has control of most front panel VCR functions such as playback, record, and forward and reverse tape motion.

3.5 Standard-Resolution Acquisition/Display and Interface

Standard RS-170 analog video signals may be digitized and are generated by an Imaging Technology, Inc (ITI) FG-100 Frame Grabber/Display board installed in the image processor system card cage. This board provides a video resolution of 480 lines by 640 8-bit pixels, with 4 bits of overlay per pixel. RGB outputs are provided, with pseudo-color available from lookup tables. These RGB outputs are connected to the standard resolution monitor for video display. Four input channels are provided by this board for digitization of RS-170 type analog video signals. One of these channels is also capable of digitizing the luminance information from an NTSC video signal. This input is used for the VCR video digitization.

The standard resolution monitor is a 13 inch diagonal measure Sony model PVM1210. This unit accepts both RS-170 RGB and NTSC analog video signals.

3.6 Model Manual Controls

Six degrees of control are required for manual manipulation of the wire-frame model displayed on the high-resolution monitor in the GADS application. This capability is provided by two 3-D joysticks where one control provides X, Y, and Z (scale) control, and the other provides yaw, pitch, and roll. X, Y, yaw, and pitch are controlled by lateral displacements on the sticks. Z and roll are controlled by rotation of knobs on the end of the sticks.

The yaw, pitch, and roll joystick is mounted on an articulated arm attached to the IDAPS operator's console. This allows the operator to position the joystick control such that the stick and knob movement will correspond in three-space to the wire-frame movements on the screen. The XYZ joystick rests directly on the operator's desk.

The joysticks used are manufactured by Measurement Systems, Inc. A joystick with an integrated RS-232 interface, Model 529Z, is used for the XYZ functions. The arm-mounted joystick is Model 526Z, mounted in an ERIM custom designed enclosure, with a Model 4302 RS-232 interface attached. Each serial interface provides periodic transmissions of data incorporating position (of the joystick) information, when the stick is displaced. These joysticks have return-to-center springs and detents. No transmissions occur with no displacement of the stick. Joystick inputs are received and utilized by the IDAPS host computer.

3.7 Host Computer System Console

The operator communicates with the host computer in IDAPS, a Digital Equipment Corporation (DEC) MicroVAX II, via a DEC VT-320 terminal. This terminal provides operator data entry, application-specific function keys, as well as system status and outputs. A formatted screen output is provided for the GADS application for ease of use.

SECTION IV

GRAPHICS SUBSYSTEM

4.1 Graphics/Display Controller

A graphics/display subsystem is integrated in IDAPS in the form of a board set within the image processor subsystem. The unit is a Univision Technologies, Inc. model UDC-3400. This unit provides variable display resolution up to a maximum 1024 lines by 1280 8-bit pixels, with 2 bits per pixel of overlay. The video memory holds up to two 1024 square images. Lookup tables are provided to display 256 colors from a pallette of 16.4 million. RS-343 60-Hz non-interlaced analog video is output for driving a high-resolution video display monitor.

The graphics engine on this board is an Intel 82786, with display-list memory of 512K bytes. Line, polygon, and bit-block transfers can be performed at high-speed. These capabilities are used to draw the wire-frame model into an overlay channel in the GADS application.

A VSB bus connection is provided on the Univision. Both the display-list and video memory are accessible from this bus. This interface is used to move images to and from the Univision and the image processor in IDAPS at high speed.

4.2 VSB Interface

The graphics subsystem provides a high-speed port for moving images into or out of the display buffer via the VSB. A VSB interface has been designed by ERIM to interface this bus to the image processor I/O interconnect for high-speed image transfers between the image processor memory and the Univision video memory.

SECTION V

IMAGE PROCESSING SUBSYSTEM

The image processing subsystem of IDAPS is the Cyto-HSS, a powerful, general purpose image processing engine emphasizing morphological and cellular processing techniques. The Cyto-HSS incorporates a recirculating pipelined architecture utilizing multiple dedicated data paths for image data movement, hardware processing elements that perform morphological, cellular, arithmetic and logical operations on images, intelligent image memory for storage and sourcing of image data for processing, a system controller that allows overlap of programming and processing for optimal speed of execution, a general-purpose CPU for additional image processing power and system control, and an Ethernet interface for communications with a host computer. The system is housed in a VMEbus card cage with slots available for other processors or peripherals (Univision graphics/display controller, ITI frame buffer, and interfaces in the IDAPS configuration).

Image processing algorithms for this hardware engine are developed in a high-level interactive programming language known as C4PL. This programming environment runs on the host computer. High-level image operations are invoked from the language as single line commands. In addition, a facility exists for calling and/or incorporating user-written routines written in standard computer programming languages (such as FORTRAN, C, or Pascal). The GADS application program is written in FORTRAN and runs under C4PL.

The Cyto-HSS image processing system in IDAPS consists of three Neighborhood Processing Stages, three 1 Megabyte Image Memories, one Combiner, one Port, the general-purpose CPU board, and an Ethernet interface board.

5.1 Neighborhood Processing Stage

The Cyto-HSS Neighborhood Processing Stage (NPS) performs a programmable 3 by 3 neighborhood transformation on incoming raster-scan ordered 8-bit pixels, producing a raster-scan stream of processed pixels at its output. Once the pipeline of stages has been programmed and filled with image data, processing occurs at a rate of 10 million 3 by 3 neighborhood transformations per second per stage. Any number of stages can be cascaded, and each stage in the pipeline can be independently programmed. Image processing capabilities can therefore be increased by cascading more stages.

The initial IDAPS incorporates three stages. Each stage is implemented on an extended-depth VMEbus form-factor printed-circuit board, and stages reside in a separate card cage from the rest of the image processing system. This card cage has

an ERIM designed backplane that implements the stage pipeline data path, and is connected to the Port and Combiner modules in the system card cage via ribbon cable.

Although there is physical space for 20 stages in the stage card cage, power supply restrictions limit the number of stages to 13 (10 stages plus 30% expansion capability).

5.2 Image Memory

Cyto-HSS Image Memories provide image storage and supply image data in raster-scan order at 10 megapixels/second to the stages and other processing elements in the system. Each image memory is capable of sourcing and receiving data for storage simultaneously. Windowing, and image resizing are also supported. All memories can supply data on any one of three source data paths (data supplied to processors) and can take in data from one of two destination data paths (data output from processors). Image data locations to access, window parameters, and data paths to use are all programmably defined prior to each processing cycle by the general-purpose CPU via the VMEbus.

Three 1-Mbyte image memory modules are provided for image storage within the image processor. Image storage space may be expanded by adding additional image memories, up to the slot space limit of the card cage. The image processor data paths are implemented on a ERIM designed printed circuit board backplane.

5.3 Combiner

The Combiner can be programmed to perform image-to-image operations which do not require neighborhood processing. The Combiner can add, multiply, mask or logically merge images. Up to three image operands can be used, selectable from the stage pipeline output and the three source image data paths. Stage pipeline output is always gated through the Combiner. Results of image operations performed by the Combiner can be placed on either (or both, in the case of operations resulting in output pixels of greater than 8-bit resolution) of the image destination paths. Programming of the Combiner is performed by the CPU via the VMEbus.

5.4 Port

The Port acts as the central control for initiating, monitoring, and halting high-speed hardware operations. It initiates hardware cycles for image processing and interrupts the general-purpose CPU to signal completion of an image processing cycle or detection of an error condition. The Port contains a data storage queue which can be loaded with port commands and stage program data for the next cycle while the current image processing cycle is in progress.

The Port serves as a gateway to the stage pipeline. Stage programming information is loaded by the CPU (across the VMEbus) into the data storage queue on the Port. Image data is fed down the pipeline by the Port from one of the three source data paths being driven by an image memory. The Combiner receives pipeline processed data.

5.5 CPU

The IDAPS hardware system controller consists of a single board VMEbus computer (Plessey model 68-31). This board has a 68030 microprocessor with a 68881 floating-point coprocessor, both operating at a clock speed of 16.7 MHz. 4 Megabytes of RAM are on board, along with full VMEbus controller functions, two RS-232 serial ports, and an interface to the VSB.

This CPU serves as local intelligence for the image processor. It responds to directions received from the host computer (via the Ethernet link described below), coordinates, initiates, and monitors all activity within the hardware system. It may also perform image processing functions not supported in hardware.

5.6 Ethernet Interface

Communications between the MicroVAX host computer and Cyto-HSS image processing hardware is accomplished via an Ethernet connection. This interface is implemented with a Communication Machinery Corporation ENP-10 board. This board incorporates its own processor to handle network functions, and has TCP/IP firmware installed.

SECTION VI

HOST COMPUTER

The IDAPS host computer is a DEC MicroVAX II. This computer supports overall system control and the C4PL algorithm development language, runs IDAPS application programs, and can be used for other processing tasks (such subsequent processing of GADS output data files).

6.1 Hardware

The DEC MicroVAX II is configured in a BA23 cabinet installed directly in the IDAPS rack. In addition to the standard TK50 cartridge tape drive, DEQNA interface, and 180 megabyte internal hard disk drive is an Emulex RS-232 I/O expansion unit that provides 16 ports in addition to the system console, and a CMC ENP-50 Ethernet interface.

The operator's terminal is connected to the MicroVAX system console port. RS-232 serial ports are used for two joysticks, VCR control, and film transport control.

6.2 Software

IDAPS system software installed on the MicroVAX includes: MicroVMS 4.7, C4PL, the GADS application programs, Decnet software, and TCP/IP for the CMC Ethernet board.

SECTION VII

SYSTEM SPECIFICATIONS

7.1 Mechanical

IDAPS is housed in standard 19-inch electronics rack. A desk is supplied for the operator console, to include the high-resolution and standard-resolution monitors, the terminal, and two joysticks. The distance between the devices on the desk and the I/O panel on the back of the rack cannot exceed about 10 feet, due to the supplied cable lengths.

Dimensions:

Desk: 60" wide by 30" deep by 48" high (including monitors)
Rack: 23" wide by 38" deep by 78" high

Weight:

Desk: 260 pounds (approximate, including all devices on the desk)
Rack: 420 pounds (approximate)

7.2 Electrical

DC Supply Ratings:

+5VDC: 150 amps at 40 degrees C
+−12VDC: 5 amps (each)

AC Requirement: 29 amps (maximum) at 120VAC

The AC requirement includes devices on the desk. An AC strip is provided to service the devices on the desk. The strip may be plugged into the convience outlet on the back of the rack. The rack is supplied with a twist-lock AC plug. A separate 30 amp 120VAC service is recommended for IDAPS, with the appropriate twist-lock receptacle.

7.3 Environmental

A controlled laboratory environment is assumed for IDAPS. Use of the equipment outside of the specified ranges may result in incorrect operation and/or equipment damage.

Temperature: 10 to 35 degrees C, operating; -25 to 60 degrees C, storage

Relative Humidity: 20 to 80 %, non-condensing